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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/600,890	08/16/2000	Seiji Shirai	P19797	6628

7055 7590 05/24/2002

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EXAMINER
DINH, TUAN T

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/600,890	Applicant(s) SHIRAI ET AL.	
	Examiner Tuan T Dinh	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 17 is objected to because of the following informalities:

Claim 17, line 4, change "then" to –them--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 9, 17, 25, line 4, it is unclear. What does applicant meant of "...layers each having formed through them holes?" Does applicant meant of "each insulative resin layer having a plurality of through holes?"

Regarding claim 1, lines 8-11, it is unclear. What does applicant meant of "for the viahole being formed substantially flat and lying in a...in which the plating also lies?" What does applicant meant of "...conductive circuit layer...insulative layer in which the plating layer also lies?"

Regarding claims 5,14,21, and 31, lines 2-3, it is unclear. What does applicant meant of "a further viahole is formed on the viahole?"

Regarding claims 7,16,23, and 32, lines 2-4, it is unclear. What does applicant meant of "the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4?" Does applicant meant of "height, thickness or length?"

Regarding claim 15, lines 2-3, it is unclear. The phrase of "the interlaminar insulative resin layer **in which** the viaholes are formed is made of a..." is not understood.

Regarding claims 4, 13, 20, lines 2-3, it is confuse. The phrase of "the surfaces of the inner conductor circuits connected to each other by the viahole are roughened" is not understood. What does applicant meant of "the surface of...circuit connected to each other?"

Regarding claim 26, line 3-4, it is unclear. The phrase of "...and thermosetting resin impregnated in the voids in the cloth" is not understood.

4. Claim 1 recites the limitation "the thickness" in line 12. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 1 recites the limitation "the surface of said plating layer" in line 7. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 1 recites the limitation "the hole" in line 7. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 1 recites the limitation "the surface of the conductive circuit" in line 9. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 2 recites the limitation "the inner wall of the hole" in line 2. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 3 recites the limitation "the conductor circuit surfaces" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 4 recites the limitation "the surfaces of inner conductor circuits" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 7 recites the limitation "the ratio" in line 2. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 9 recites the limitation "the thickness" in 6. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 10 recites the limitation "the inner hole" in line 2. There is insufficient antecedent basis for this limitation in the claim.

14. Claim 11 recites the limitation "the central surface portion" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

15. Claim 12 recites the limitation "the plating layer surface and conductor circuit surface" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

16. Claim 13 recites the limitation "the surfaces of the inner conductor circuits" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 27 recites the limitation "the inner wall of the hole" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

19. Claims 17-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Kinoshita (U. S. Patent 6,294,744).

As best understood to claims 17, 21, Kinoshita discloses a multilayer printed wiring board (100-figure 1) and also shown in figures 2-6 having conductor circuitry layers (3) and interlaminar insulative resin layers (4) deposited alternately one on another, the interlaminar insulative resin layers each having formed holes (5) each filled with a plating layer (7) to form a viahole, characterized by:

said hole having an inner wall thereof roughened (see figure 3D);

said roughened inner wall being covered with a roughened electroless plating layer (see figures 3D-3F); and

an inner space of said hole defined by the electroless plating layer and filled with an electroplating layer.

As to claims 18-20, Kinoshita discloses a multilayer printed wiring board as shown in figures 2-6 wherein depressions are formed in the central surface portion of the plating layer surface exposed out of the hole

As to claim 22, Kinoshita discloses a multilayer printed wiring board as shown in figures 2-6 wherein the interlaminar insulative resin layer in which in viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

As best understood to claim 23, Kinoshita discloses a multilayer printed wiring board as shown in figures 2-6 wherein the ratio between the viahole diameter and a thickness of interlaminar insulative resin layer is within a range of 1 to 4.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 1-16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita (U. S. Patent 6,294,744).

As best understood to claims 1, 4-5, 8-9, 13-14, 24, Kinoshita discloses a multilayer printed wiring board (100-figure 1) and also shown in figures 2-4 having conductor circuitry layers (3, 3a-figure 3A, column 4, line 24) and interlaminar insulative resin layers (4-figure 3B, column 4, line 39) deposited alternately one on another, the interlaminar insulative resin layers each having formed holes (5, column 5, line 23) each filled with a plating layer (7, column 4, line 53) to form a viahole, characterized by:

the surface of said plating layer (7) exposed out of the hole for the viahole (5) being formed substantially flat and lying in a substantially same level as the surface of the conductor circuit layer (see figure 2) disposed in the interlaminar insulative resin layer (4); and

Kinoshita shows said viahole having a diameter less than 25 micrometers (column 4, lines 59-61). Kinoshita does not show a thickness of said conductor circuitry layer being less than a half of the viahole diameter.

It would well known to one having ordinary skill in the art at the time the invention was made to have a thickness of said conductor circuitry layer being less than a half of the viahole diameter to employ the structure of the multiplayer printed wiring board of Kinoshita in order to provide an improvement of finer ultra circuit pattern on the printed wiring board, since has been held discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

As best understood to claims 2, 10, Kinoshita discloses a multilayer printed wiring board as shown in figures 3D-3F) wherein an inner wall of the hole is roughened (column 4, line 52, column 6, lines 34-44).

As best understood to claims 3, 11-12, Kinoshita discloses a multilayer printed wiring board as shown in figures 2-6 wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole are roughened.

As to claims 6, 15, Kinoshita discloses a multilayer printed wiring board as shown in figures 1-6 wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins (liquid resin 4a, column 4, line 41).

As best understood to claims 7, 16, Don discloses a multilayer printed wiring board wherein the ratio between the viahole diameter and a thickness of interlaminar insulative resin layer is within a range of 1 to 4 (column 4, lines 60-61, column 5, lines 21-22).

22. Claims 25-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita (U. S. Patent 6,294,744) in view of Takenouchi et al. (U. S. Patent 5,744,758).

As best understood to claims 25-33, Kinoshita discloses all of the limitations of the claimed invention, except for an interlaminar insulative layer being formed of a composite of thermosetting resin and heat-resistant thermoplastic resin.

Takenouchi shows a multiplayer printed wiring board (10) as shown in figures 1-10 comprising an interlaminar insulative layer being formed of a composite of thermosetting resin and heat-resistant thermoplastic resin (14, 16, column 5, line 67, and column 6, lines 1-5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an interlaminar insulative layer being formed of a composite of thermosetting resin and heat-resistant thermoplastic resin as taught by Takenouchi to employ the interlaminar insulative layer of Kinoshita in order to improve an electro-conductivity and provide thermal-expansion or contraction rates between materials constituting of a multiplayer printed wiring board and vias.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Enomoto et al., Frankeny et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD
May 19, 2002.

KAMAND CUNEO
PRIMARY EXAMINER